

**AMENDMENTS TO THE CLAIMS:**

1. (Currently Amended) A device (100)—arranged to compose basic-code vectors (102a, 102b up to and including 102n)—into a composite-code vector (104), the device (100) comprising:

at least two weighted sum units (106a, 106b), each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors (102a, 102b up to and including 102n);

an add unit (110), the add unit being arranged to sum the intermediate-code vectors into the composite-code vector (104);

the weighted sum units (106a, 106b)—being under the control of a first and a second configuration word (114a, 114b), and

wherein the first and the second configuration word (114a, 114b)—are deployed to configure the operations performed by the weighted sum units.

2. (Currently Amended) A device (100)—according to claim 1, wherein a pre-processing unit (108a, 108b)—is coupled to at least one of the weighted sum units (106a, 106b)—and to the add unit (110), the pre-processing unit (108a, 108b)—being arranged to perform additional operations on the intermediate-code vector, and the pre-processing unit (108a, 108b)—being under the control of a third and a fourth configuration word (116a, 116b), wherein the third and the fourth configuration word (116a, 116b)—are deployed to configure the additional operations on the intermediate-code vector.

3. (Currently Amended) A device (100)—according to claim 1, wherein a post-processing unit (112) is coupled to the add unit (110), the post-processing unit (112) being arranged to perform additional operations on the composite-code vector (104), and the post-processing unit (112) being under the control of a fifth configuration word (118), wherein the fifth configuration word (118) is deployed to configure the additional operations on the composite-code vector.
4. (Currently Amended) A device (100)—according to claim 1, wherein the weighted sum units (106a, 106b) are arranged to calculate a bit-wise addition of at least two basic-code vectors (102a, 102b up to and including 102n).
5. (Currently Amended) A device (100)—according to claim 2, wherein the pre-processing unit (108a, 108b) is arranged to erase, repeat and reorder the elements of the intermediate-code vector.
6. (Currently Amended) A device (100)—according to claim 2, wherein the pre-processing unit (108a, 108b) is arranged to apply a mask on the intermediate-code vector.
7. (Currently Amended) A device (100)—according to claim 3, wherein the post-processing unit (112) is arranged to perform a conditional negation of the composite-code vector (104).

8. (Currently Amended) A device (100) according to claim 1, wherein the weighted sum units (106a, 106b) and the add unit (110) are arranged to be configured during a configuration stage of the operation of the device-(100).
9. (Currently Amended) A device (100) according to claim 2, wherein the pre-processing unit (108a, 108b) is arranged to be configured during a configuration stage of the operation of the device-(100).
10. (Currently Amended) A device (100) according to claim 3, wherein the post-processing unit (112) is arranged to be configured during a configuration stage of the operation of the device-(100).

11. (Currently Amended) A method for composing basic-code vectors (102a, 102b up to and including 102n) into a composite-code vector (104), the method comprising the steps of:

- (a) providing, by a vector processor, a first and a second intermediate-code vector, each of which is a weighted sum of a plurality of the basic-code vectors (102a, 102b up to and including 102n);
- (b) summing, by the vector processor, the intermediate-code vectors into a composite-code vector (104);
- (c) providing receiving, by the vector processor, a first and a second configuration word (114a, 114b); and
- (d) controlling, by the vector processor, step (a) with the first and the second configuration word (114a, 114b).